

# FMND4GXXX3F

3V/1.8V, x8/x16 4G-BIT NAND FLASH

***Dosilicon***

**Documents title**

4Gbit (512Mx8Bit, 256Mx16Bit) NAND FLASH

**Revision History**

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Nov 15, 2019	
0.1	Modify read ID tables	Dec 03, 2019	
0.2	Add block0 is valid block description	Jan 17, 2020	
0.3	Update tREA time	Jul 10, 2020	
0.4	Add automotive/AEC-Q100 grade2 info	Dec 3, 2021	

**FEATURES****■ x8/x16 I/O BUS**

- NAND Interface
- ADDRESS / DATA Multiplexing

**■ SUPPLY VOLTAGE**

- VCC = 1.8/2.7/3.3 Volt core supply voltage for Program, Erase and Read operations

**■ PAGE READ / PROGRAM**

- x8 : (4096+256 spare) byte
- x16: (2048+128 spare) word page
- Synchronous Page Read Operation
- Random access :           25us (Max)
- Serial access :           30ns (1.8V)  
                                  20ns (2.7/3.0V)
- Page program time :    200us (Typ)

**■ PAGE COPY BACK**

- Fast data copy without external buffering

**■ CACHE PROGRAM**

- Internal buffer to improve the program throughput

**■ READ CACHE****■ LEGACY/ONFI 1.0 COMMAND SET****■ FAST BLOCK ERASE**

- Block size :  
    x8 : (256K + 16K) bytes  
    x16: (128K + 8K) words
- Block erase time : 2ms (Typ)

**■ MEMORY CELL ARRAY**

- x8 : (4K + 256) bytes x 64 pages x 2048 blocks
- x16: (2K + 128) words x 64 pages x 2048 blocks

**■ ELECTRONIC SIGNATURE**

- Manufacturer Code
- Device Code

**■ STATUS REGISTER****■ HARDWARE DATA PROTECTION****■ DATA RETENTION**

- 100K Program / Erase cycles
- Data retention : 10 Years(4bit/512byte ECC)
- Block zero is a valid block and will be valid for at least 1K program-erase cycles with ECC

## Part Numbering System

**F M N D X X X X X X - X X**

### Dosilicon Memory

#### Product Family

ND : NAND

#### Density

28 : 128Mb  
56 : 256Mb  
12 : 512Mb  
1G : 1Gb  
2G : 2Gb  
4G : 4Gb  
8G : 8Gb  
6G : 16Gb

#### Organization

08 : x8  
16 : x16

#### Operation Voltage

U : 3.3V  
L : 2.5V  
S : 1.8V

#### Package Type

0 : Bare Die  
W : KGD  
A : 12 x 20 mm<sup>2</sup> (TSOP1 48) H-ROHS & Halogen Free  
B : 12 x 17 mm<sup>2</sup> (ULGA 52) H-ROHS & Halogen Free  
C : 9 x 9 mm<sup>2</sup> (48 FBGA) H-ROHS & Halogen Free  
D : 9 x 11 mm<sup>2</sup> (63 FBGA) H-ROHS & Halogen Free  
F : 6.5 x 8 mm<sup>2</sup> (67 FBGA) H-ROHS & Halogen Free

#### Temperature

C : Commercial (0°C~70°C)  
E : Extended (-25°C~85°C)  
I : Industrial (-40°C~85°C)  
A2 : Automotive/AEC-Q100 Grade2  
(-40°C~105°C)

#### Generation

F

#### Classification

1 : SLC S/B  
2 : MLC S/B  
3 : SLC L/B  
4 : MLC L/B

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## 1 SUMMARY DESCRIPTION

**FMND4GXXX3F** is a **512Mx8bit** with spare **32Mx8 (x8)**, **256Mx16bit** with spare **16Mx16(x16)** bit capacity.

The device is offered in 3.3/1.8 Vcc Power Supply, and with x8 and x16 I/O interface.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains **2048 blocks**, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. Program operation allows the 4352-byte page writing in typical 200us and an erase operation can be performed in typical **2 ms** on a 256K-byte block.

Data in the page can be read out at **20ns** cycle time per word (**2.7/3V version**), and at **30ns** cycle time per word (**1.8V version**). The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.

The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP# input pin.

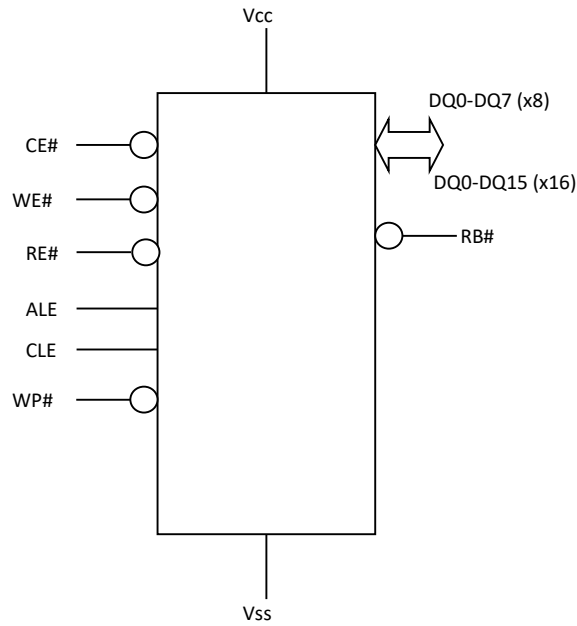
This device supports ONFI 1.0 specification.

The output pin RB# (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the RB# pins can be connected all together to provide a global status signal.

The **FMND4GXXX3F** is available in the following packages : 48 - TSOP1 12x20 mm package, FBGA63 9x11 mm.

### 1.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE
FMND4G08S3F	X8	1.7 – 1.95 Volt	VFBGA, TSOP
FMND4G16S3F	X16	1.7 – 1.95 Volt	VFBGA, TSOP
FMND4G08L3F	X8	2.5 – 3.0 Volt	VFBGA, TSOP
FMND4G16L3F	X16	2.5 – 3.0 Volt	VFBGA, TSOP
FMND4G08U3F	X8	2.7 – 3.6 Volt	VFBGA, TSOP
FMND4G16U3F	X16	2.7 – 3.6 Volt	VFBGA, TSOP



**Figure 1:** Logic Diagram

DQ7 - DQ0	Data Input / Outputs (x8/x16)
DQ15 – DQ8	Data Input / Outputs (x16)
CLE	Command latch enable
ALE	Address latch enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
RB#	Ready / Busy
Vcc	Power supply
Vss	Ground
NC	No Connection

**Table 1:** signal names

## 1.2 Pin description

Pin Name	Description
<b>DQ0-DQ7(x8) DQ0-DQ15(x16)</b>	DATA INPUTS/OUTPUTS The DQ pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE#). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
<b>CLE</b>	COMMAND LATCH ENABLE This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
<b>ALE</b>	ADDRESS LATCH ENABLE This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
<b>CE#</b>	CHIP ENABLE This input controls the selection of the device. When the device is busy CE# low does not deselect the memory.
<b>WE#</b>	WRITE ENABLE This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
<b>RE#</b>	READ ENABLE The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid $t_{REA}$ after the falling edge of RE# which also increments the internal column address counter by one.
<b>WP#</b>	WRITE PROTECT The WP# pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
<b>RB#</b>	READY BUSY The Ready/Busy output is an Open Drain pin that signals the state of the memory.
<b>Vcc</b>	SUPPLY VOLTAGE The VCC supplies the power for all the operations (Read, Write, Erase). An internal lock circuit prevent the insertion of Commands when V <sub>CC</sub> is less than V <sub>LKO</sub>
<b>Vss</b>	GROUND
<b>NC / DNU</b>	NOT CONNECTED / DON'T USE

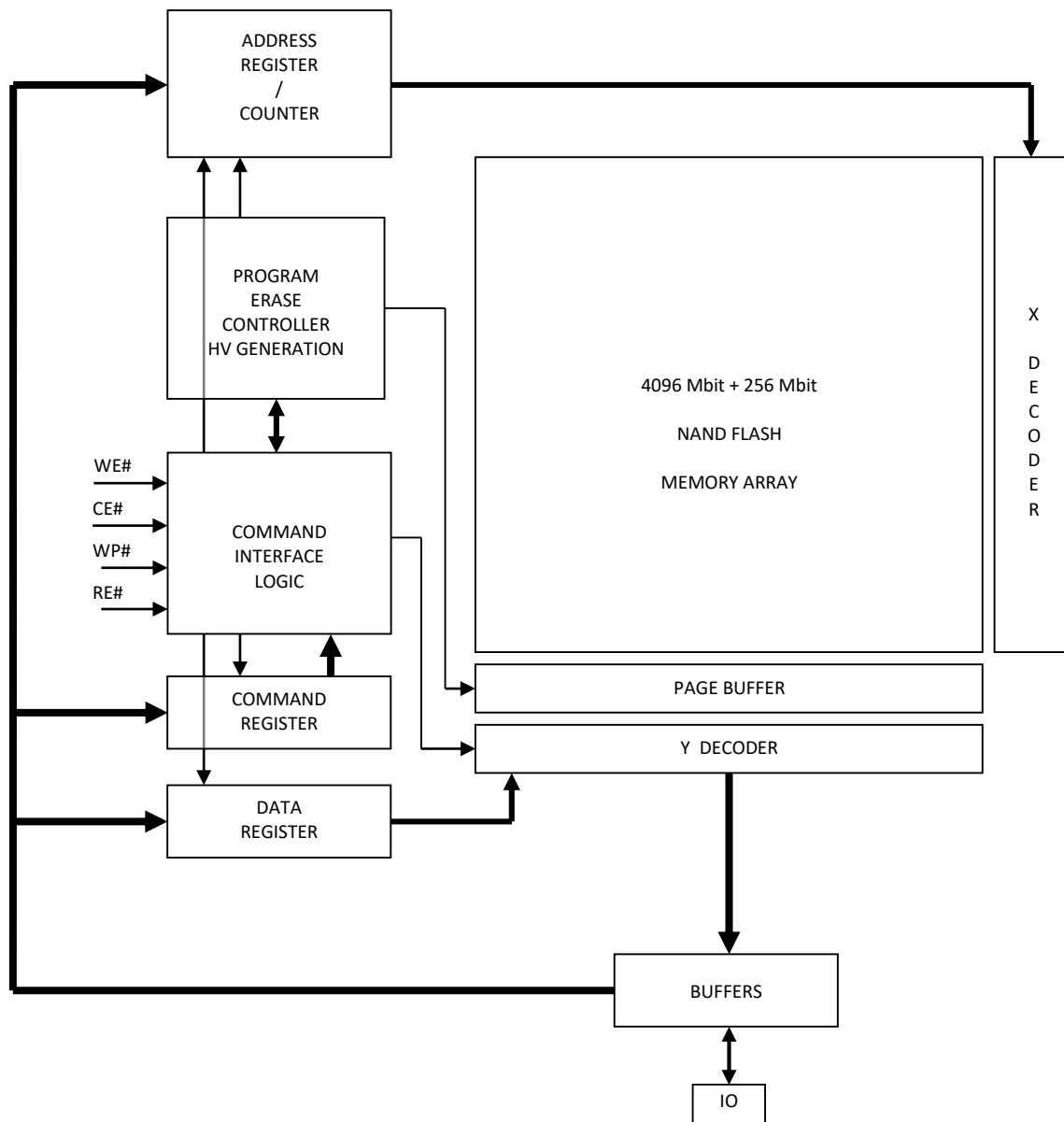
**Table 2** : pin description

Notes:

1. A 0.1  $\mu$ F capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.



### 1.3 Functional block diagram



**Figure 2** : block description

## 1.4 Address role

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1 <sup>st</sup> Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2 <sup>nd</sup> Cycle	A8	A9	A10	A11	A12	0	0	0
3 <sup>rd</sup> Cycle	A13	A14	A15	A16	A17	A18	A19	A20
4 <sup>th</sup> Cycle	A21	A22	A23	A24	A25	A26	A27	A28
5 <sup>th</sup> Cycle (*)	A29	A30	0	0	0	0	0	0

**Table 3** : Address Cycle Map (x8)

(\*): A30 for 8Gbit DDP.

A0 – A12 : byte (column) address in the page

A13 – A18 : page address in the block

A19 – A30 : block address

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1 <sup>st</sup> Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2 <sup>nd</sup> Cycle	A8	A9	A10	A11	0	0	0	0
3 <sup>rd</sup> Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4 <sup>th</sup> Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5 <sup>th</sup> Cycle (*)	A28	A29	0	0	0	0	0	0

**Table 4** : Address cycle Map (x16)

(\*): A29 for 8Gbit DDP.

A0 – A11 : word (column) address in the page

A12 – A17 : page address in the block

A18 – A29 : block address

## 1.5 Command Set

FUNCTION	1 <sup>st</sup> CYCLE	2 <sup>nd</sup> CYCLE	3 <sup>rd</sup> CYCLE	4 <sup>th</sup> CYCLE	Acceptable command during busy
READ	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PGM (start) / CACHE PGM (end)	80h	10h	-	-	
CACHE PGM (Start/continue)	80h	15h	-	-	
COPY BACK PGM	85h	10h	-	-	
BLOCK ERASE	60h	D0h	-	-	
READ STATUS REGISTER	70h	-	-	-	Yes
READ STATUS ENHANCED	78h				Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
READ CACHE (SEQUENTIAL)	31h				
READ CACHE ENHANCED (RANDOM)	00h	31h	-	-	
READ CACHE END	3Fh	-	-	-	
READ PARAMETER PAGE	ECh				
EXTENDED READ STATUS	F2h/F3h	-	-	-	Yes

**Table 5 : Command Set**

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L <sup>(1)</sup>	H	Falling	X	Data Output (on going)	
X	X	L <sup>(1)</sup>	H	H	X	Data Output (suspended) <sup>(2)</sup>	
L	L	L	H	H	X	Busy time in Read	
X	X	X	X	X	H	Busy time in Program	
X	X	X	X	X	H	Busy time in Erase	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V / V <sub>CC</sub>	Stand By	

**Table 6 : Mode Selection**

## **2 BUS OPERATION**

### **2.1 Command Input.**

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 3 and Table 21 for details of the timings requirements. Command codes are always applied on IO<7:0>, disregarding the bus configuration (X8/X16).

### **2.2 Address Input.**

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 4 and Table 21 for details of the timings requirements. Addresses are always applied on IO<7:0>, disregarding the bus configuration (X8/X16).

### **2.3 Data Input.**

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 5 and Table 21 for details of the timings requirements.

### **2.4 Data Output.**

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 6,7,8 and Table 21 for details of the timings requirements.

### **2.5 Write Protect.**

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

### **2.6 Standby.**

In Standby the device is deselected, outputs are disabled and Power Consumption reduced.

## 3 DEVICE OPERATION

### 3.1 Page Read.

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing **00h** and **30h** to the command register along with **5** address cycles. In two consecutive read operations, the second one does need 00h command, which four address cycles and **30h** command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.

Two types of operations are available: random read , serial page read. The random read mode is enabled when the page address is changed. The **4352** bytes (X8 device) or **2176** words (X16 device) of data within the selected page are transferred to the data registers in less than **25us(tR)**. The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in **20ns cycle time (3V version) or 30ns cycle time (1.8V version)** by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command.

The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

Any operation other than read or random data output causes device to exit read mode.

Check Figure 10,11,12 as references.

### 3.2 Read Cache

The Read Cache function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in **3.1**, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence.

The Read Cache function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read.

Figure 13 defines the Read Cache behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. Figure 14 defines the Read Cache behavior and timings for the end of cache operation.

### 3.3 Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 4352 (X8 device) or words up to 2176 (X16 device), in a single page program cycle.

A page program cycle consists of a serial data loading period in which up to **4352 bytes** (X8 device) or **2176 words** (X16 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (**80h**), followed by **5** cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (**85h**). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (**10h**) initiates the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 15,16 detail the sequence.

### 3.4 Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "**35h**" command and the address of the source page moves the whole 4352byte (X8 device) or 2176word (X16 device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (**85h**) with the address cycles of destination page may be written. The Program Confirm command (**10h**) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 17.

### 3.5 Cache Program

Cache Program is an extension of the standard page program which is executed with two 4352 bytes(x8 device) or 2176 words(x16 device) registers, the data and the cache register.

In short, the cache program allows data insertion for one page while program of another page is under execution. Cache program is available only within a block.

After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register.

Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time ( $t_{PCBSY}$ ). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).

The busy time following the first sequence 80h – 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence 80h – 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state ( $t_{PCBSY}$ ).

Read Status commands (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. It is represented in Figure 18.

More in detail:

- a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
  - b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete
  - c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1".
  - d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1".
- I/O<1> may be read together with I/O<0>.

If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

### 3.6 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in **3** cycles initiated by an Erase Setup command (**60h**). The Erase Confirm command (**D0h**) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

**Figure** details the sequence..

### 3.7 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing **70h** command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when RB# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to Table 7 for specific Status Register definitions, and Figure 8 for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (**00h**) should be given before starting read cycles.

### 3.8 Read Status Register field definition

Table 7 below lists the meaning of each bit of Read Status Register and Read Status Enhanced

IO	Page Program	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass/Fail	N page Pass: '0' Fail: '1'
1	NA	NA	NA	NA	Pass/Fail	N-1page Pass: '0' Fail: '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Active: '0' Idle: '1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data cache Read/Busy Busy: '0' Ready: '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

**Table 7 : Status Register Coding**

### 3.9 Read ID.

The device contains a product identification mode, initiated by writing **90h** to the command register, followed by an address input of 00h.

DENSITY	ORG.	VCC	1 <sup>st</sup>	2 <sup>nd</sup>	3 <sup>rd</sup>	4 <sup>th</sup> (1)	5 <sup>th</sup>
4Gbit	X8	3.0V	F8h	DCh	80h	A6h	62h
	X16	3.0V	00F8h	CCh	80h	E6h	62h
	X8	1.8V	F8h	ACh	80h	26h	62h
	X16	1.8V	00F8h	BCh	80h	66h	62h
8Gbit DDP	X8	3.0V	E5h	D3h	C1h	A6h	66h
	X16	3.0V	00E5h	C3h	C1h	E6h	66h
	X8	1.8V	E5h	A3h	C1h	26h	66h
	X16	1.8V	00E5h	B3h	C1h	66h	66h

**Table 8:** Read ID for supported configurations

DEVICE IDENTIFIER BYTE	DESCRIPTION
1 <sup>st</sup>	Manufacturer Code
2 <sup>nd</sup>	Device Identifier
3 <sup>rd</sup>	Internal chip number, cell type,....
4 <sup>th</sup>	Page Size, Block Size, Spare Size, Organization
5 <sup>th</sup>	Multiplane information

**Table 9 :** Read ID bytes meaning

	Description	DQ7	DQ6	DQ5-4	DQ3-2	DQ1-0
Internal Chip Number	1					0 0
	2					0 1
	4					1 0
	8					1 1
Cell Type	2 Level Cell				0 0	
	4 Level Cell				0 1	
	8 Level Cell				1 0	
	16 Level Cell				1 1	
Number of simultaneously programmed pages	1			0 0		
	2			0 1		
	4			1 0		
	8			1 1		
Interleaved program between multiple dice	Not Supported		0			
	Supported		1			
Cache Program	Not Supported	0				
	Supported	1				

**Table 10 :** 3<sup>rd</sup> byte of Device Identifier Description



	Description	DQ7	DQ6	DQ5-4	DQ3	DQ2	DQ1-0
Page Size (Without Spare Area)	1KB						0 0
	2KB						0 1
	4KB						1 0
	8KB						1 1
Spare Area Size (Byte / 512 Byte)	16					0	
	32					1	
Block Size (Without Spare Area)	64KB			0 0			
	128KB			0 1			
	256KB			1 0			
	512KB			1 1			
Organization	X8		0				
	X16		1				
Serial Access Time	50ns/30ns	0			0		
	20ns	1			0		
	Reserved	0			1		
	Reserved	1			1		

**Table 11 : 4<sup>th</sup> Byte of Device Identifier Description**

	Description	DQ7	DQ6-4	DQ3-2	DQ1-0
ECC Level	1bit/512Byte				0 0
	2bit/512Byte				0 1
	4bit/512Byte				1 0
	8bit/512Byte				1 1
Plane Number	1			0 0	
	2			0 1	
	4			1 0	
	8			1 1	
Plane Size (Without Spare Area)	64Mb		0 0 0		
	128Mb		0 0 1		
	256Mb		0 1 0		
	512Mb		0 1 1		
	1Gb		1 0 0		
	2Gb		1 0 1		
	4Gb		1 1 0		
	8Gb		1 1 1		
Reserved		0			

**Table 12 : 5<sup>th</sup> Byte of Device Identifier Description**

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 20 shows the operation sequence .

### 3.10 Reset.

The device offers a reset feature, executed by writing **FFh** to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to Table 7 for device status after

reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for  $t_{RST}$  after the Reset command is written (see Figure 22).

### 3.11 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. Figure 23 defines the Read Parameter Page behavior.

Values in the parameter page are static and shall not change. The host is not required to read the parameter page after power management events.

The Change Read Column command can be issued during execution of the Read Parameter Page to read specific portions of the parameter page.

Read Status may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

### 3.12 Parameter Page Data Structure Definition

Table 14 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data *bytes* are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.

For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Byte	O/M	Description
<b>Revision information and features block</b>		
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache 18ntegrit 0 1 = supports Page Cache Program command
10-31		Reserved (0)
<b>Manufacturer information block</b>		
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code

Byte	O/M	Description
67-79		Reserved (0)
<b>Memory organization block</b>		
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
<b>Electrical parameters block</b>		
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	$t_{\text{PROG}}$ Maximum page program time ( $\mu\text{s}$ )
135-136	M	$t_{\text{BERS}}$ Maximum block erase time ( $\mu\text{s}$ )
137-138	M	$t_{\text{R}}$ Maximum page read time ( $\mu\text{s}$ )
139-163		Reserved (0)
<b>Vendor block</b>		
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC

Byte	O/M	Description
<b>Redundant Parameter Pages</b>		
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

**Table 14** : Parameter page data

Note : “O” stands for Optional, “M” for Mandatory

## 4 Device Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number, 4Gb	N <sub>VB</sub>	2008	-	2048	Blocks

**Table 15:** Valid Blocks Number

The First block (Block 0) is guaranteed to be a valid block at the time of shipment.  
The specification for the minimum number of valid blocks is applicable over lifetime.

Symbol	Parameter	Value			Unit
		1.8V	2.7V	3.0V	
T <sub>A</sub>	Ambient Operating Temperature	0 to 70	0 to 70	0 to 70	°C
	Ambient Operating Temperature	-40 to 85	-40 to 85	-40 to 85	°C
	Ambient Operating Temperature	-40 to 105	-40 to 105	-40 to 105	°C
T <sub>BIAS</sub>	Temperature Under Bias	-50 to 125	-50 to 125	-50 to 125	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	-65 to 150	-65 to 150	°C
V <sub>IO</sub> <sup>(2)</sup>	Input or Output Voltage	-0.6 to 2.7	-0.6 to 4.6	-0.6 to 4.6	V
V <sub>CC</sub>	Supply Voltage	-0.6 to 2.7	-0.6 to 4.6	-0.6 to 4.6	V

**Table 16:** Absolute maximum ratings

Parameter		Symbol	Test Conditions	1.8V			2.7V			3.0V			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I <sub>CC1</sub>	t <sub>RC</sub> = 50ns, CE#=V <sub>IL</sub> , I <sub>OUT</sub> =0mA	-	10	20	-	15	30	-	15	30	mA
	Program	I <sub>CC2</sub>	-	-	10	20	-	15	30	-	15	30	mA
	Erase	I <sub>CC3</sub>	-	-	10	20	-	15	30	-	15	30	mA
Stand-by Current (TTL)		I <sub>CC4</sub>	CE#=V <sub>IH</sub> , WP#=0V/V <sub>CC</sub>	-	-	1	-	-	1	-	-	1	mA
Stand-By Current (CMOS)		I <sub>CC5</sub>	CE#=V <sub>CC</sub> -0.2, WP#=0/V <sub>CC</sub>	-	10	50	-	10	50	-	10	50	uA
Input Leakage Current		I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>C</sub> (max)	-	-	±10	-	-	±10	-	-	±10	uA
Output Leakage Current		I <sub>LO</sub>	V <sub>OUT</sub> =0 to V <sub>CC</sub> (max)	-	-	±10	-	-	±10	-	-	±10	uA
Input High Voltage		V <sub>IH</sub>	-	0.8x V <sub>CC</sub>	-	V <sub>CC</sub> +0.3	0.8x V <sub>CC</sub>	-	V <sub>CC</sub> +0.3	0.8x V <sub>CC</sub>	-	V <sub>CC</sub> +0.3	V

Input Low Voltage	$V_{IL}$	-	-0.3	-	$0.2 \times V_{CC}$	-0.3	-	$0.2 \times V_{CC}$	-0.3	-	$0.2 \times V_{CC}$	V
Output High Voltage Level	$V_{OH}$	$I_{OH} = -100\mu A$	$V_{CC} - 0.1$	-	-	$V_{CC} - 0.4$	-	-				V
		$I_{OH} = -400\mu A$							2.4	-	-	V
Output Low Voltage Level	$V_{OL}$	$I_{OL} = 100\mu A$	-	-	0.1	-	-	0.4				V
		$I_{OL} = 2.1mA$							-	-	0.4	V
Output Low Current (RB#)	$I_{OL}$ (RB#)	$V_{OL} = 0.1V$	3	4	-	3	4	-				mA
		$V_{OL} = 0.4V$							8	10	-	mA

**Table 17:** DC and Operating Characteristics

Parameter	Value		
	1.8Volt	2.7Volt	3.0Volt
Input Pulse Levels	0V to $V_{CC}$	0V to $V_{CC}$	0V to $V_{CC}$
Input Rise and Fall Times	5ns	5ns	5ns
Input and Output Timing Levels	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$
Output Load (1.7V – 1.95V & 2.5V - 3.6V)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF

**Table 18:** AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance (1)	$C_{I/O}$	$V_{IL} = 0V$	-	10	pF
Input Capacitance (1)	$C_{IN}$	$V_{IN} = 0V$	-	10	pF

**Table 19 :** Pin Capacitance (TA = 25C, f=1.0MHz)

**NOTE:** For the stacked devices version the Input Capacitance is **10pF x <number of stacked chips>** and the I/O capacitance is **10pF x <number of stacked chips>**

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		$t_{PROG}$	-	200	700	us
Cache program short busy time		$t_{PCBSY}$		3.5	$t_{PROG}$	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	TBD	Cycle
Block Erase Time		$t_{BERS}$	-	2.0	10	ms
Read Cache busy time		$t_{RCBSY}$		3.5	$t_R$	us

**Table 20:** Program / Erase Characteristics

Parameter	Symbol	1.8 Volt		2.7 Volt		3.0 Volt		Unit
		Min	Max			Min	Max	
CLE Setup time	t <sub>CLS</sub>	10		10		10		ns
CLE Hold time	t <sub>CLH</sub>	5		5		5		ns
CE# Setup time	t <sub>CS</sub>	25		15		15		ns
CE# Hold time	t <sub>CH</sub>	5		5		5		ns
WE# Pulse width	t <sub>WP</sub>	15		10		10		ns
ALE Setup time	t <sub>ALS</sub>	10		10		10		ns
ALE Hold time	t <sub>ALH</sub>	5		5		5		ns
Data Setup time	t <sub>DS</sub>	10		7		7		ns
Data Hold time	t <sub>DH</sub>	5		5		5		ns
Write Cycle time	t <sub>WC</sub>	30		20		20		ns
WE# High Hold time	t <sub>WH</sub>	10		7		7		ns
Address to Data Loading time	t <sub>ADL</sub>	100		70		70		ns
Data Transfer from Cell to Register	t <sub>R</sub>		25		25		25	us
ALE to RE# Delay	t <sub>AR</sub>	10		10		10		ns
CLE to RE# Delay	t <sub>CLR</sub>	10		10		10		ns
Ready to RE# Low	t <sub>RR</sub>	20		20		20		ns
RE# Pulse Width	t <sub>RP</sub>	15		10		10		ns
WE# High to Busy	t <sub>WB</sub>		100		100		100	ns
Read Cycle Time	t <sub>RC</sub>	30		20		20		ns
RE# Access Time	t <sub>REA</sub>		30		20		20	ns
CE# Access Time	t <sub>CEA</sub>		45		25		25	ns
RE# High to Output Hi-Z	t <sub>RHZ</sub>		100		100		100	ns
CE# High to Output Hi-Z	t <sub>CHZ</sub>		30		30		30	ns
CE# High to ALE or CLE Don't care	t <sub>CSD</sub>	10		10		10		ns
RE# High to Output Hold	t <sub>RHOH</sub>	15		15		15		ns
RE# Low to Output Hold	t <sub>RLOH</sub>	-		5		5		ns
CE# High to Output Hold	t <sub>COH</sub>	15		15		15		ns
RE# High Hold Time	t <sub>REH</sub>	10		7		7		ns
Output Hi-Z to RE# Low	t <sub>IR</sub>	0		0		0		ns
RE# High to WE# Low	t <sub>RHW</sub>	100		100		100		ns
WE# High to RE# Low	t <sub>WHR</sub>	60		60		60		ns
Device Resetting Time (Read/Program/Erase)	t <sub>RST</sub>		5/10/ 500 (1)		5/10/ 500 (1)		5/10/ 500 (1)	us
Write protection time	t <sub>WW</sub>	100		100		100		ns

Table 21 : AC Timing Characteristics

**NOTE:**

(1) If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us

## 5 Timing Diagrams

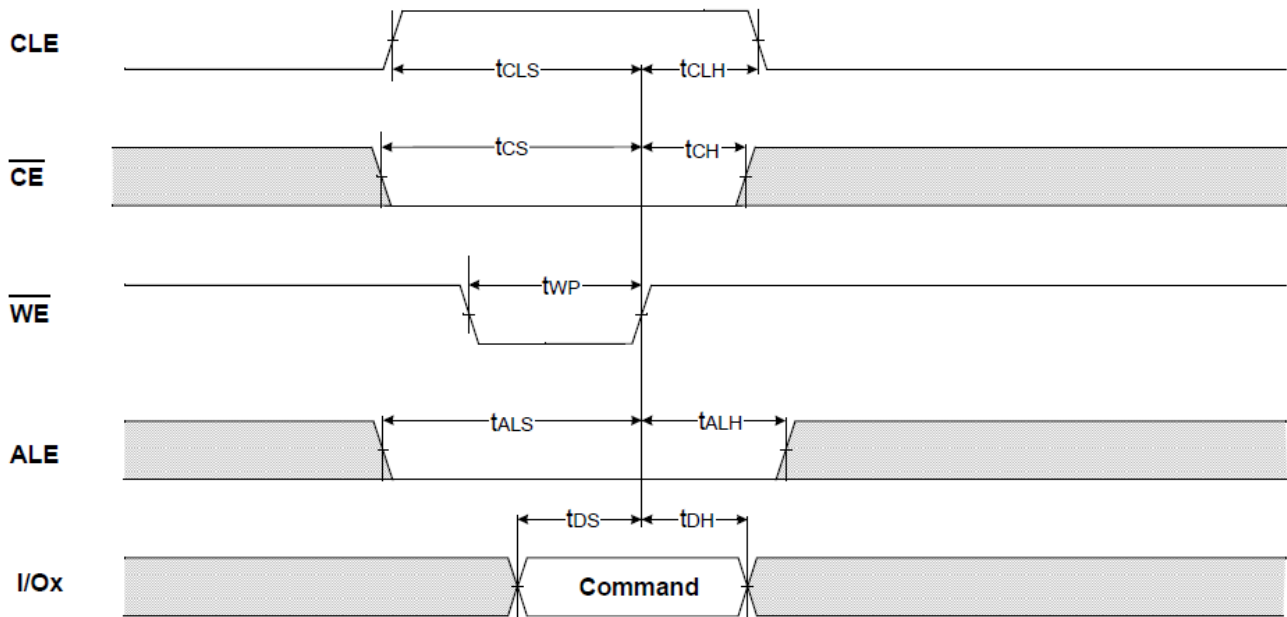


Figure 3 : Command Latch Cycle

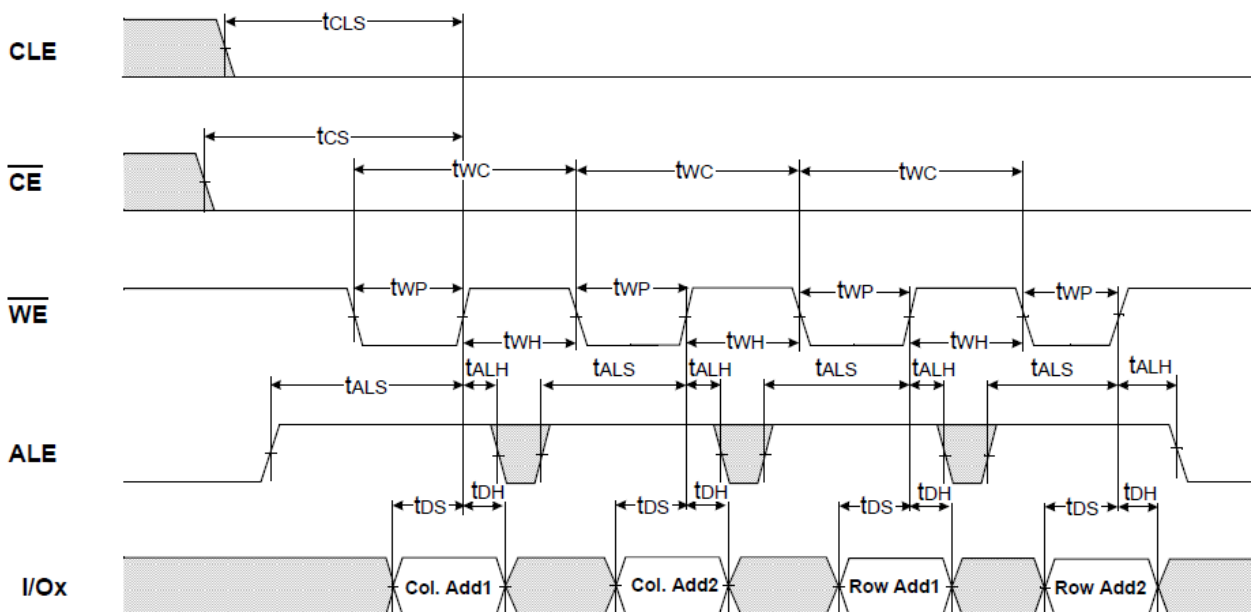
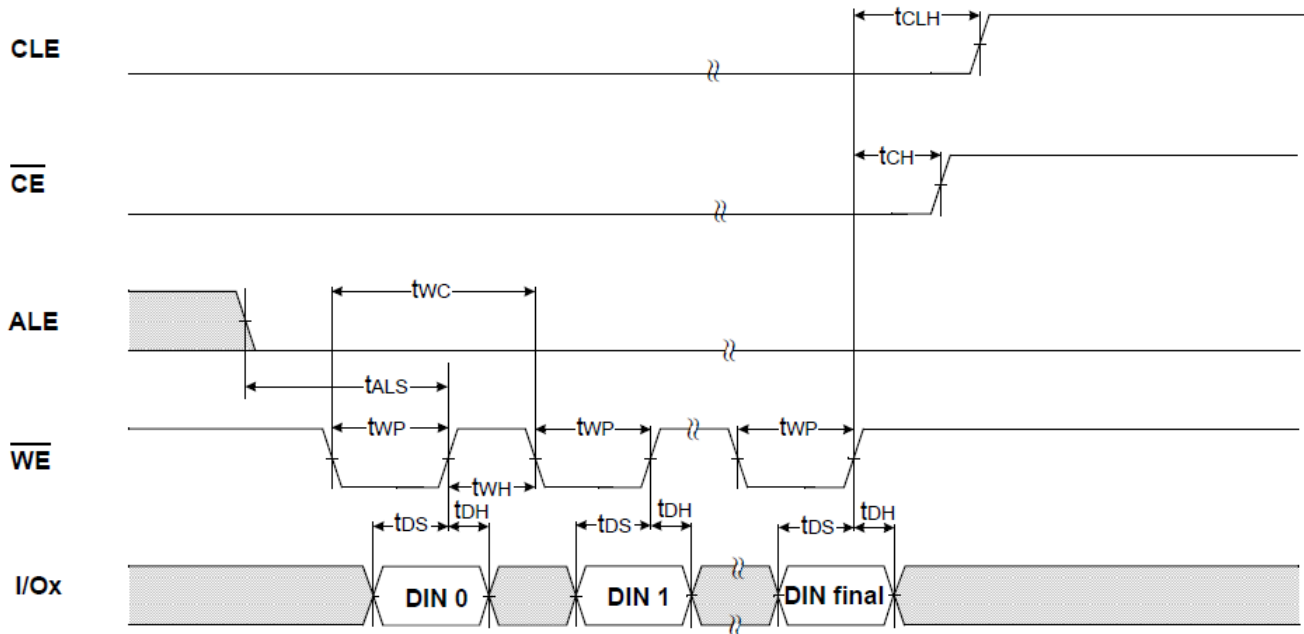
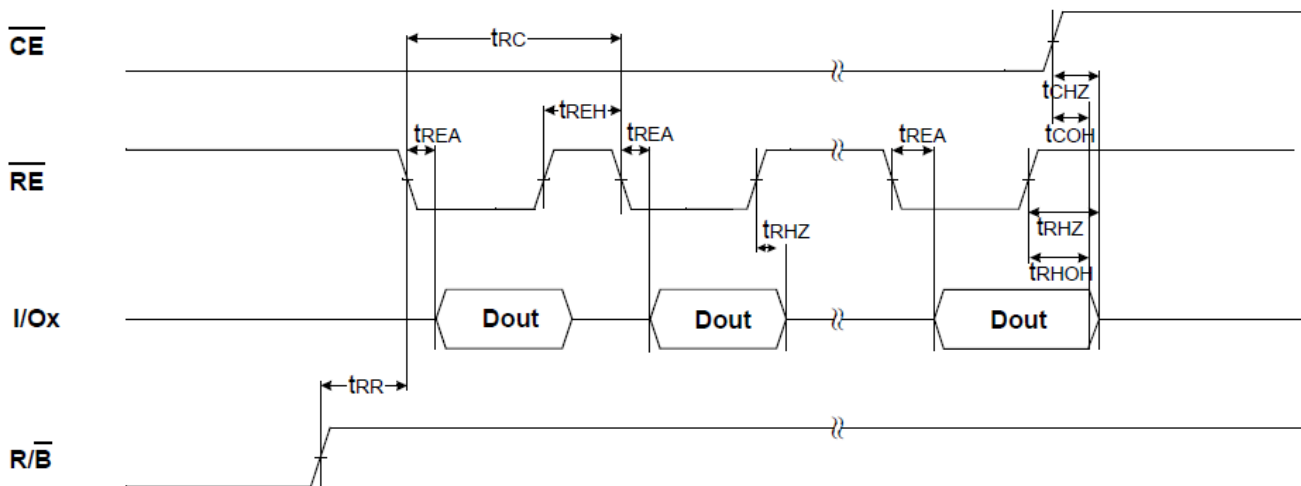


Figure 4 : Address Latch Cycle



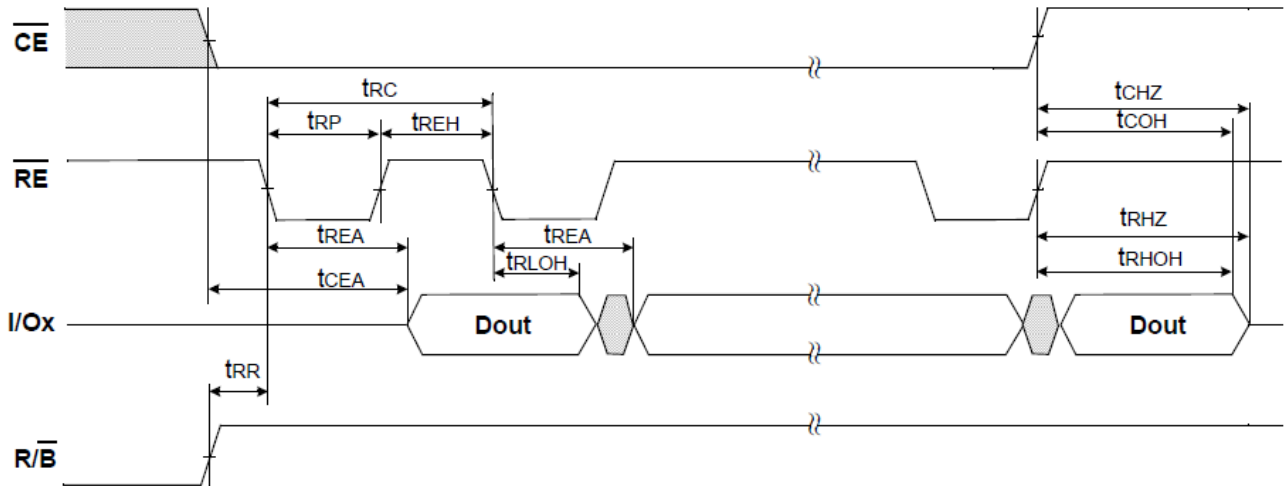
**Figure 5 : Input Data Latch Cycle**



**NOTES :** Transition is measured at  $\pm 200\text{mV}$  from steady state voltage with load.  
 This parameter is sampled and not 100% tested.  
 tRLOH is valid when frequency is higher than 33MHz.  
 tRHOH starts to be valid when frequency is lower than 33MHz.

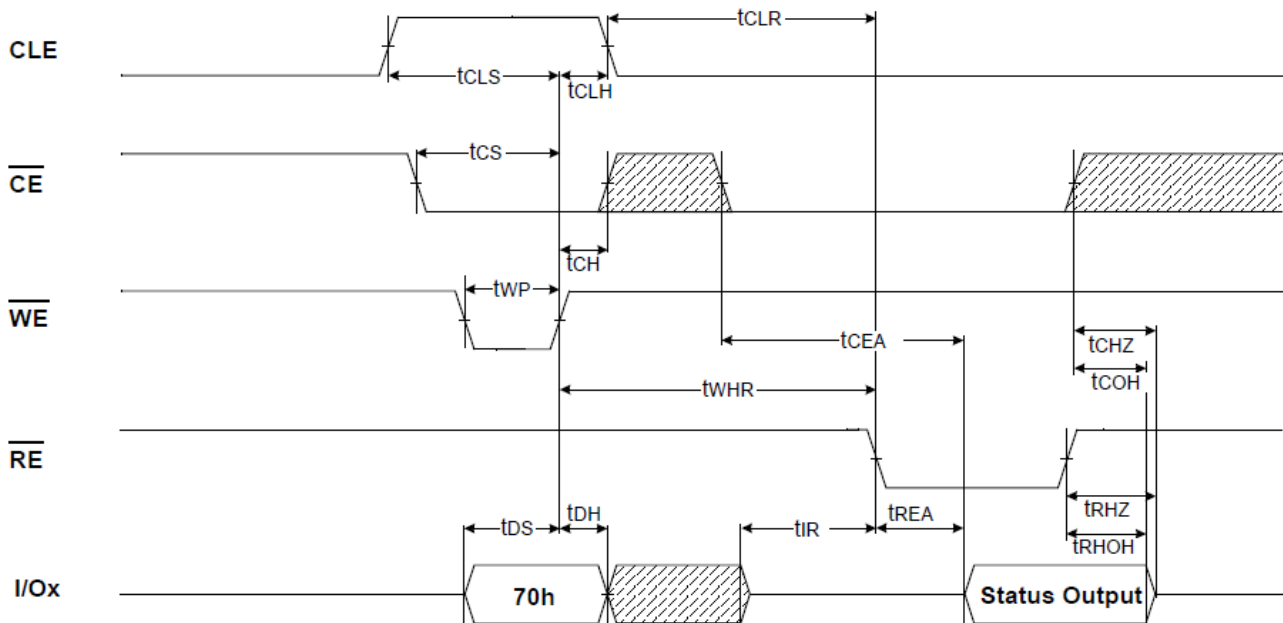
**Figure 6 : Sequential Out Cycle after Read**





**NOTES :** Transition is measured at  $\pm 200\text{mV}$  from steady state voltage with load.  
 This parameter is sampled and not 100% tested.  
 tRLOH is valid when frequency is higher than 33MHz.  
 tRHOH starts to be valid when frequency is lower than 33MHz.

**Figure 7 : Sequential Out Cycle after Read**



**Figure 8 : Status Read Cycle**

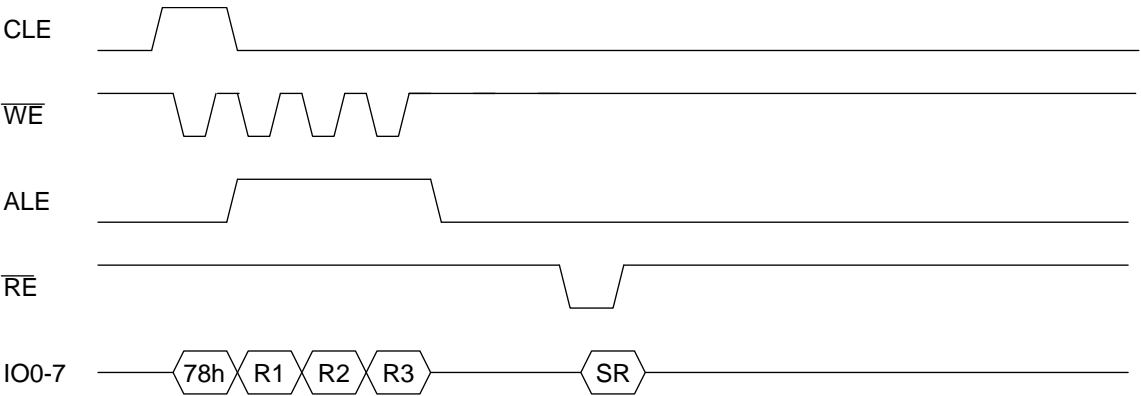


Figure 9: Read Status Enhanced cycle

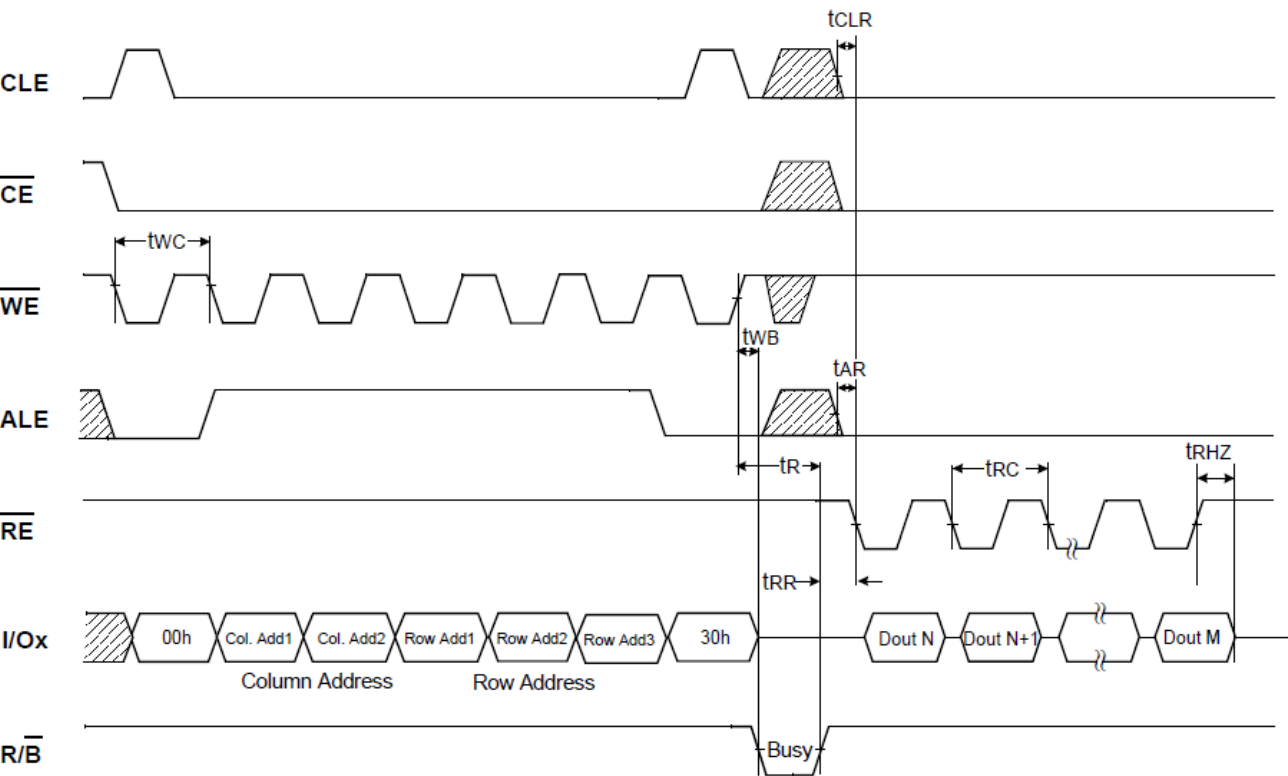


Figure 10 : Read Operation (Read One Page)

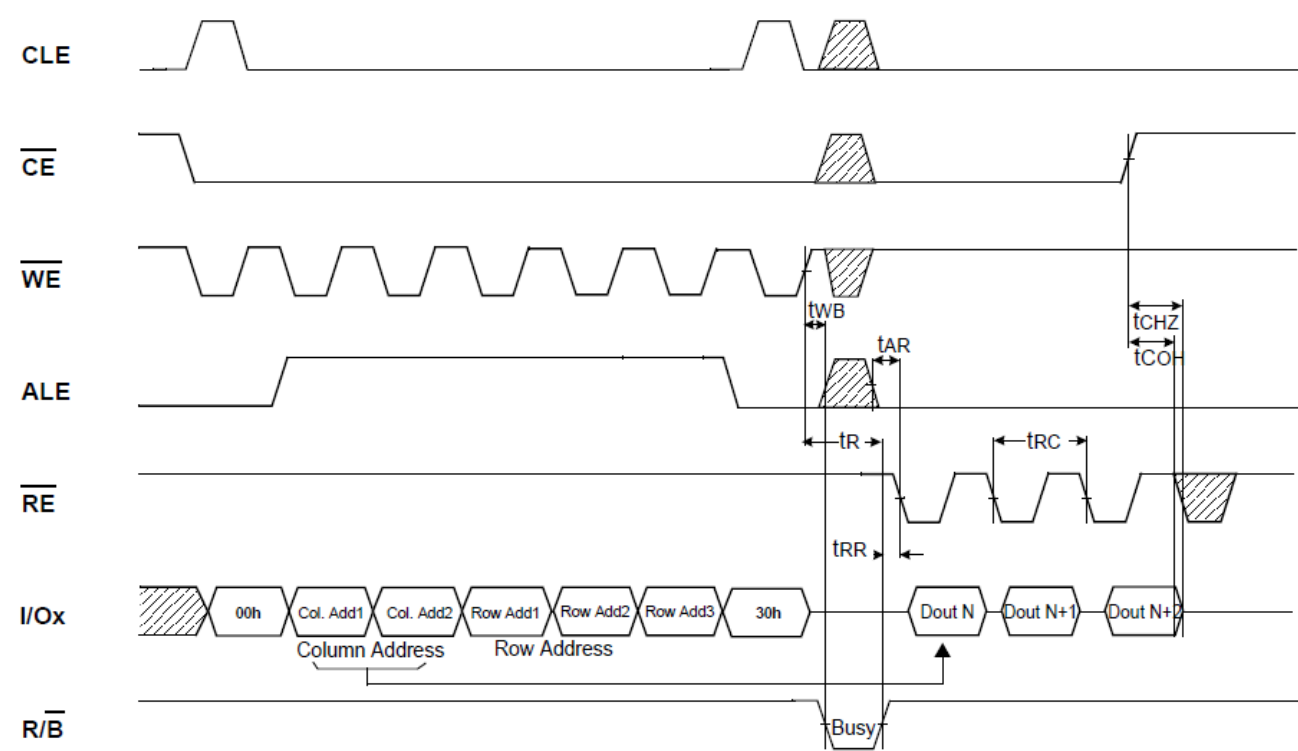


Figure 11 : Read Operation intercepted by CE#

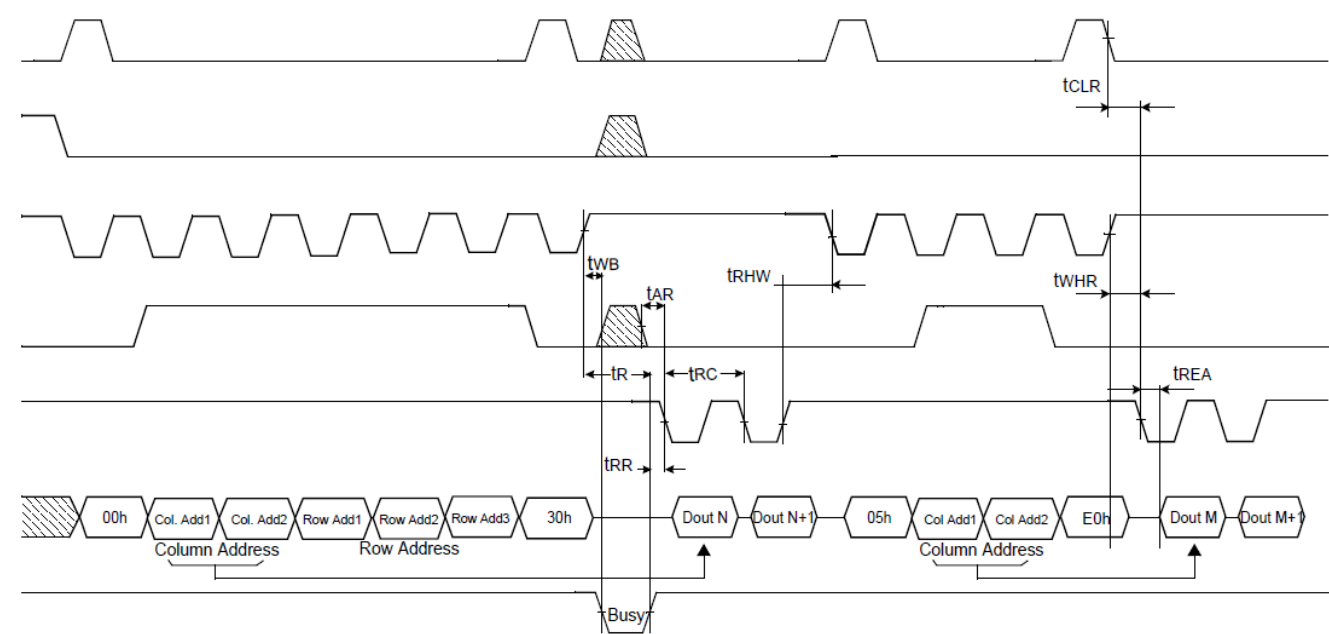
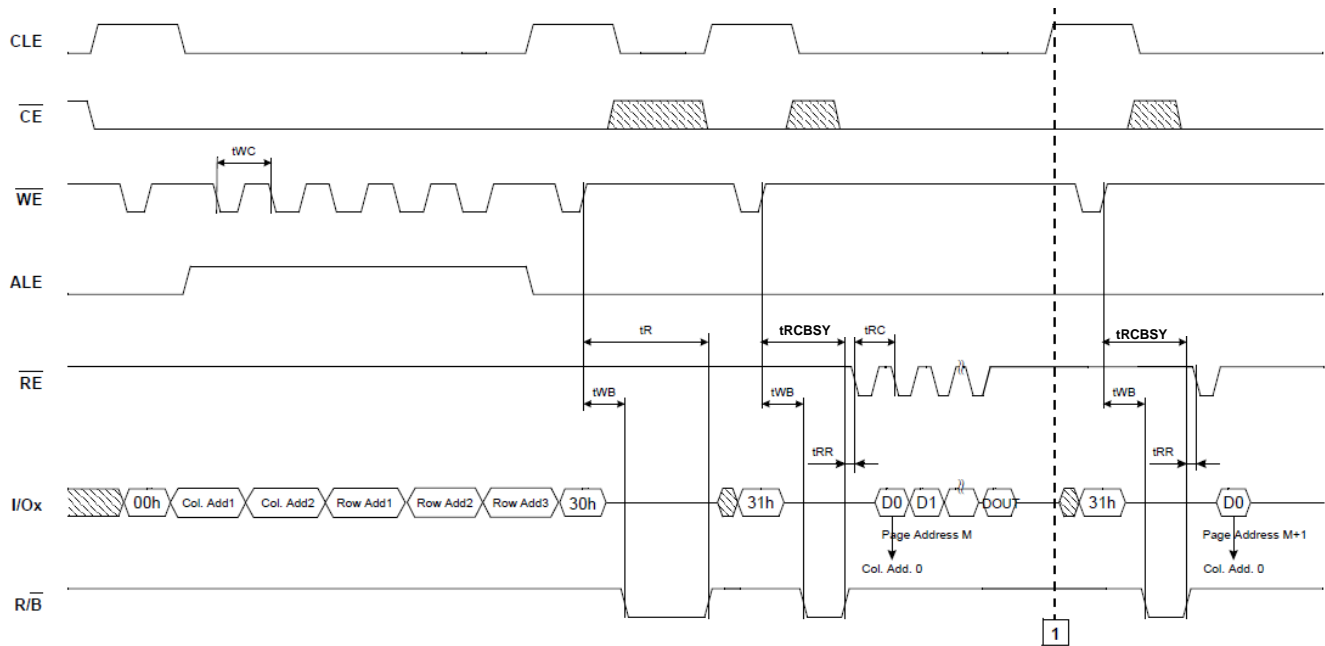
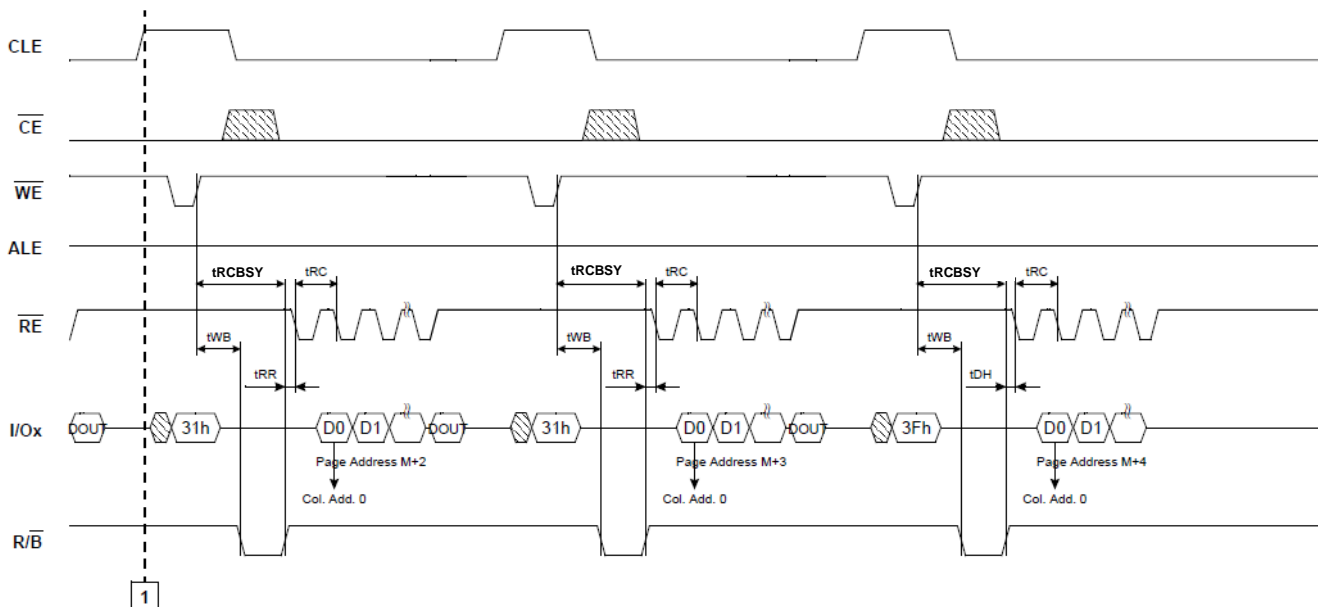


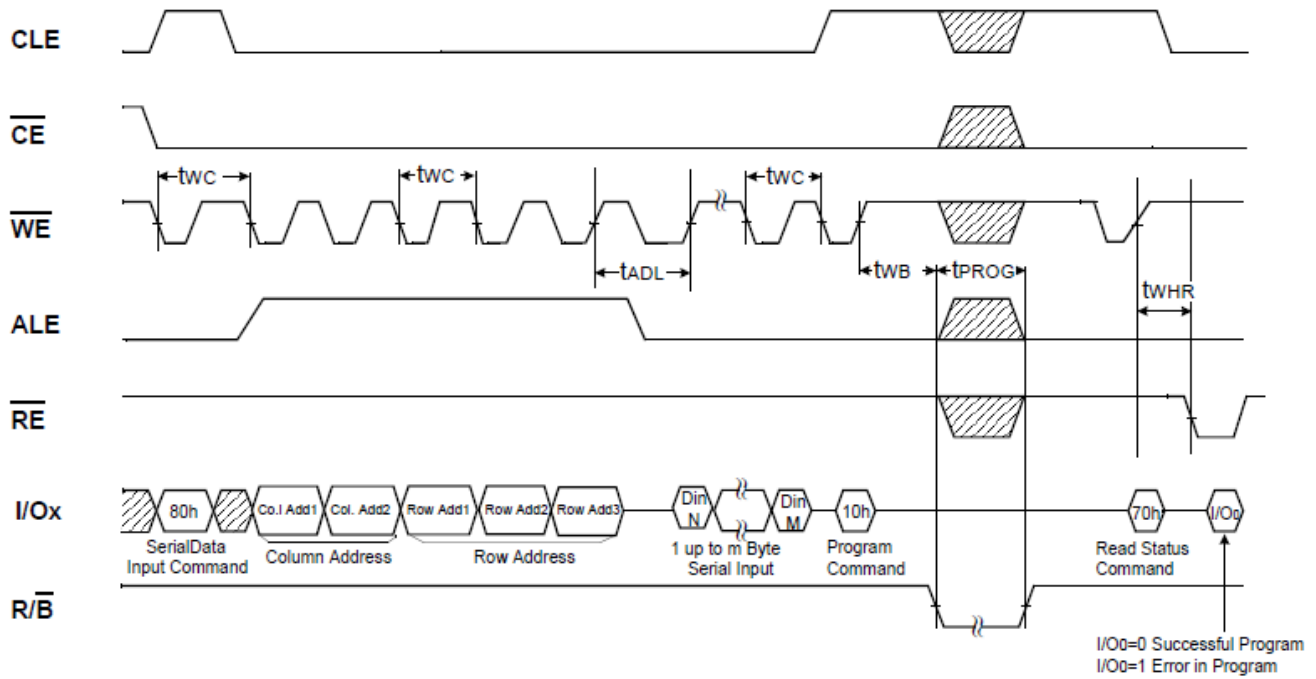
Figure 12 : Random Data Output



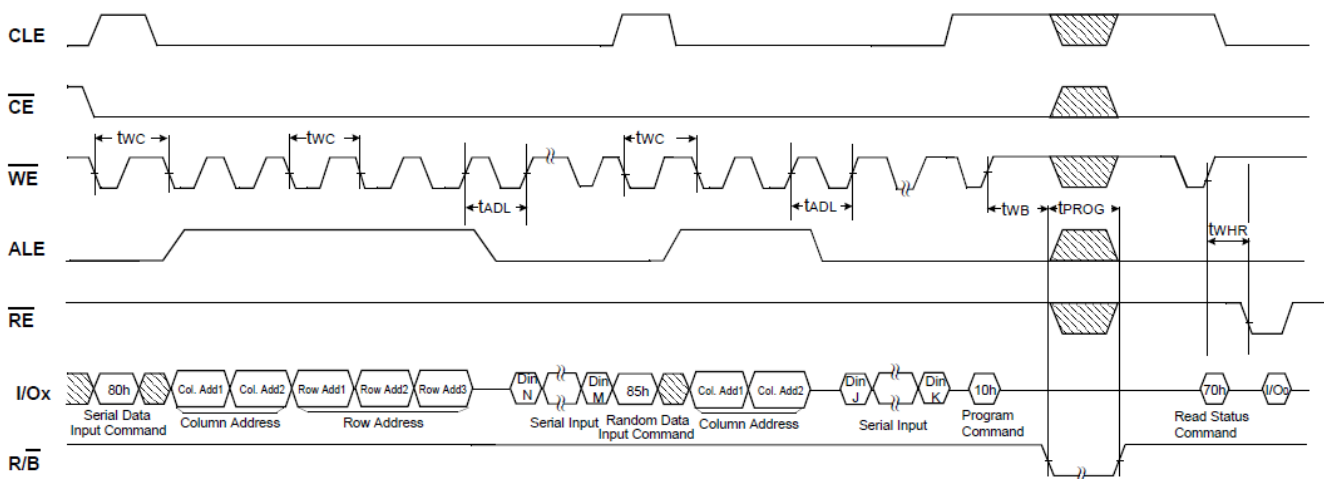
**Figure 13 : read cache timings, start of cache operation**



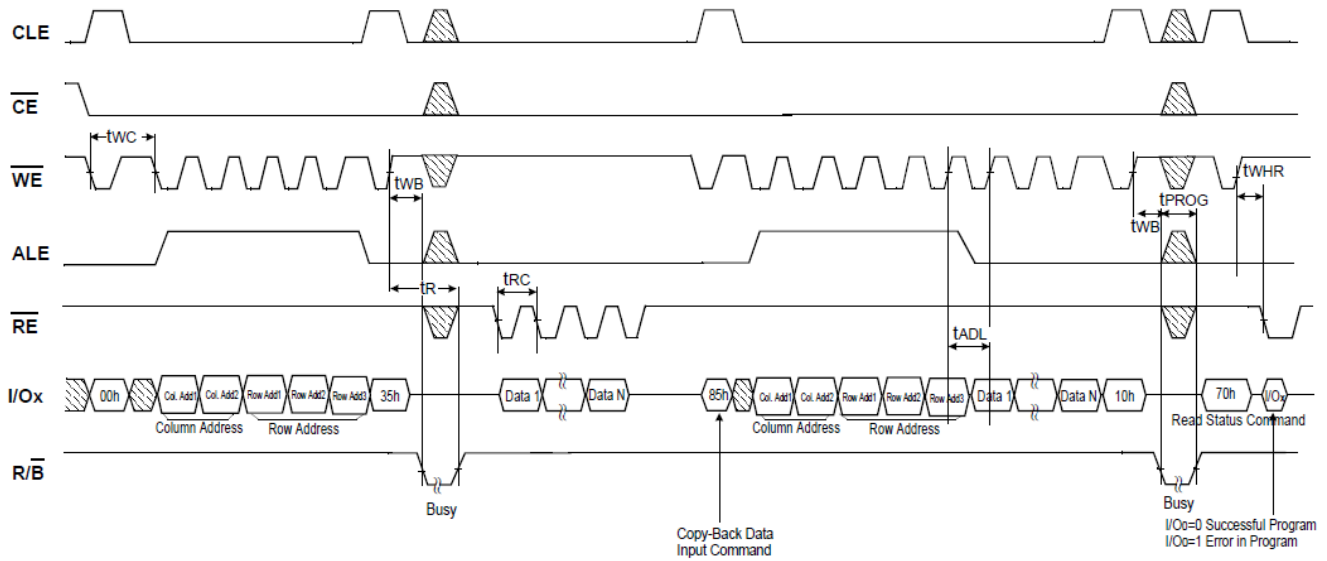
**Figure 14 : read cache timings, end of cache operation**



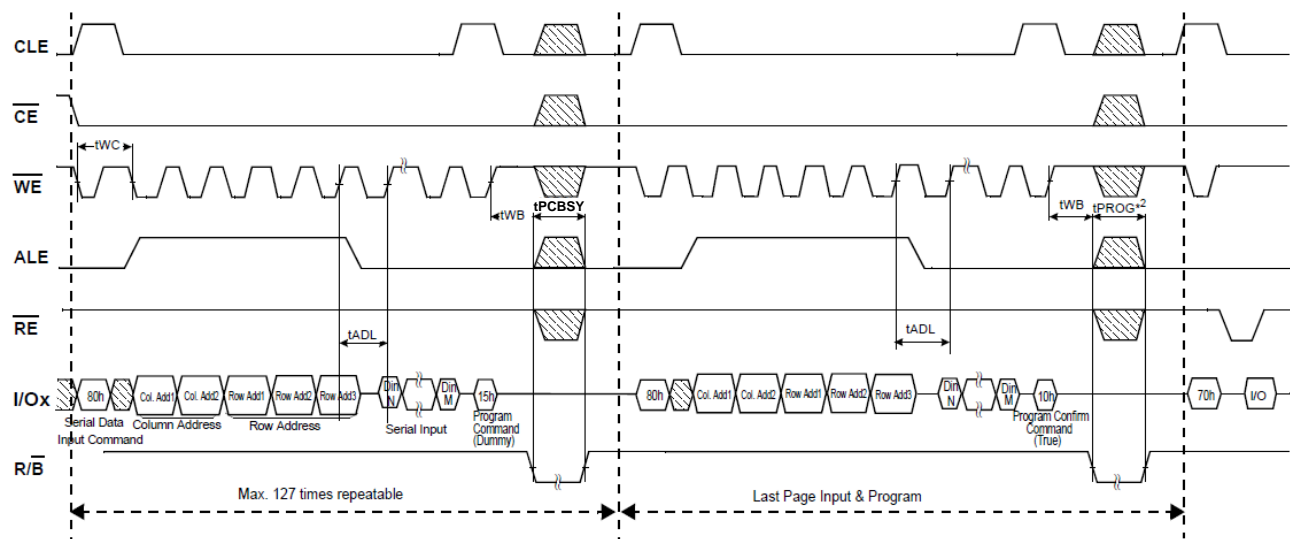
**Figure 15 : Page Program Operation**



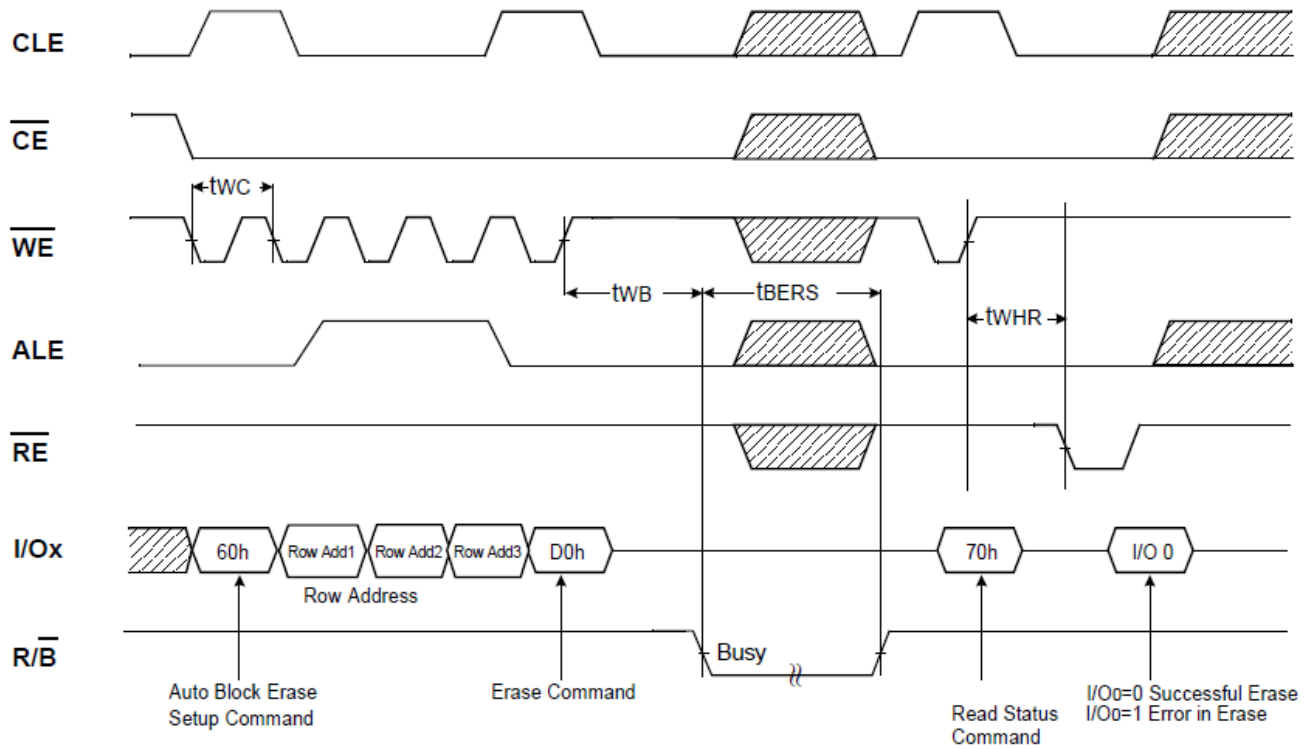
**Figure 16 : Random Data In**



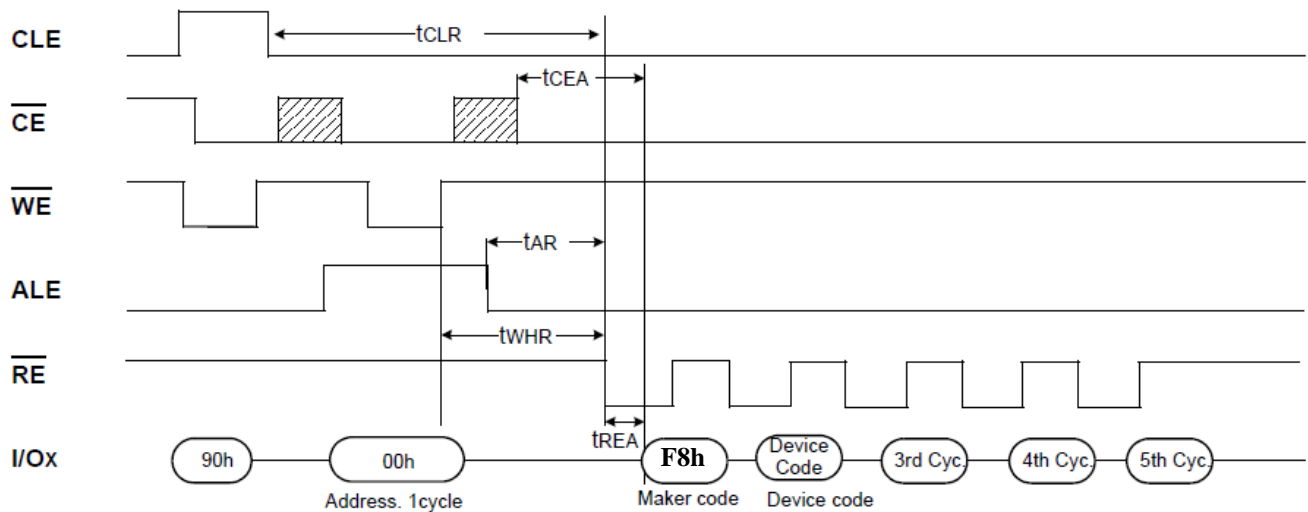
**Figure 17 :** Copy Back read with optional data readout /Copy back program with optional data input



**Figure 18 :** cache program



**Figure 19 : Block Erase Operation (Erase One Block)**



**Figure 20 : READ ID Operation**

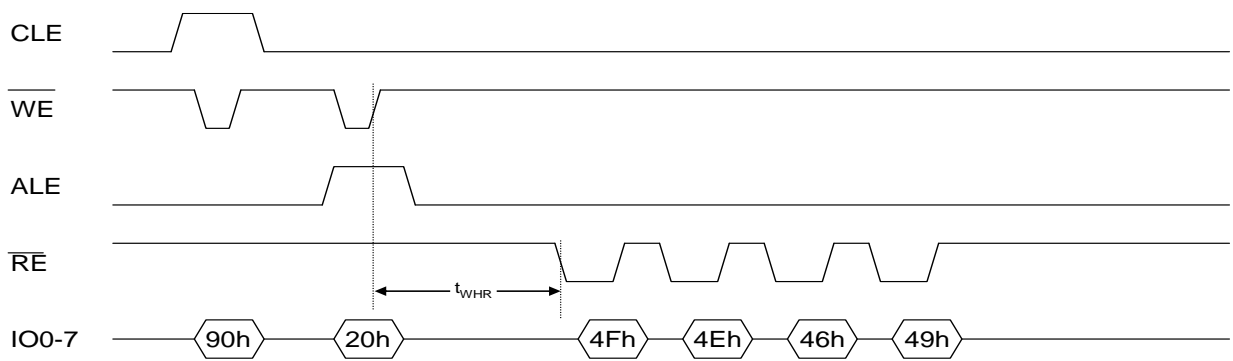


Figure 21 : ONFI signature timing diagram

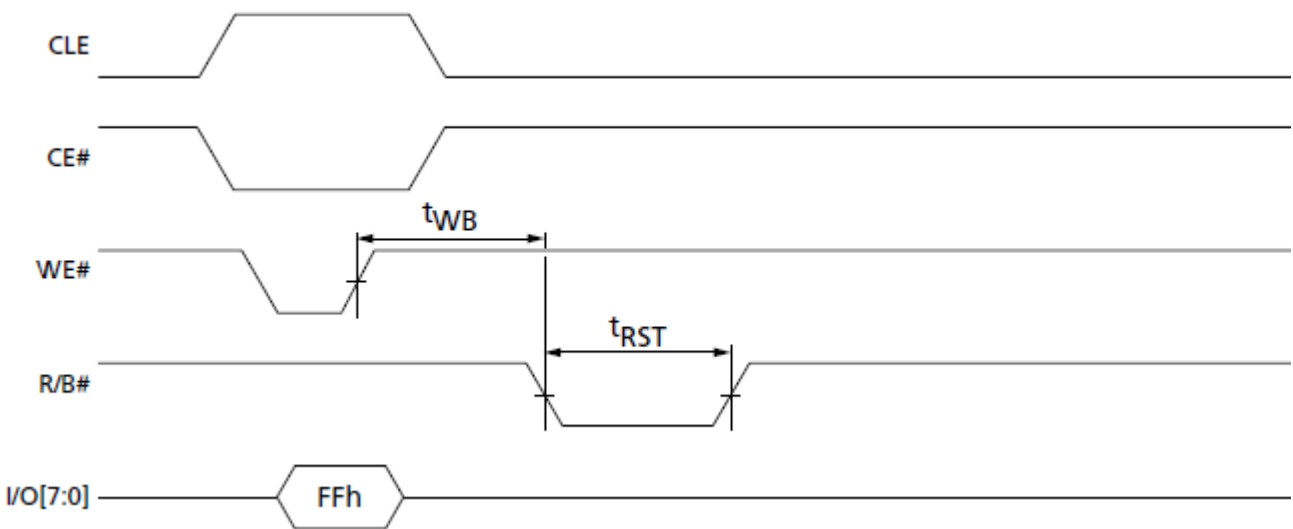


Figure 22 : Reset operation timing



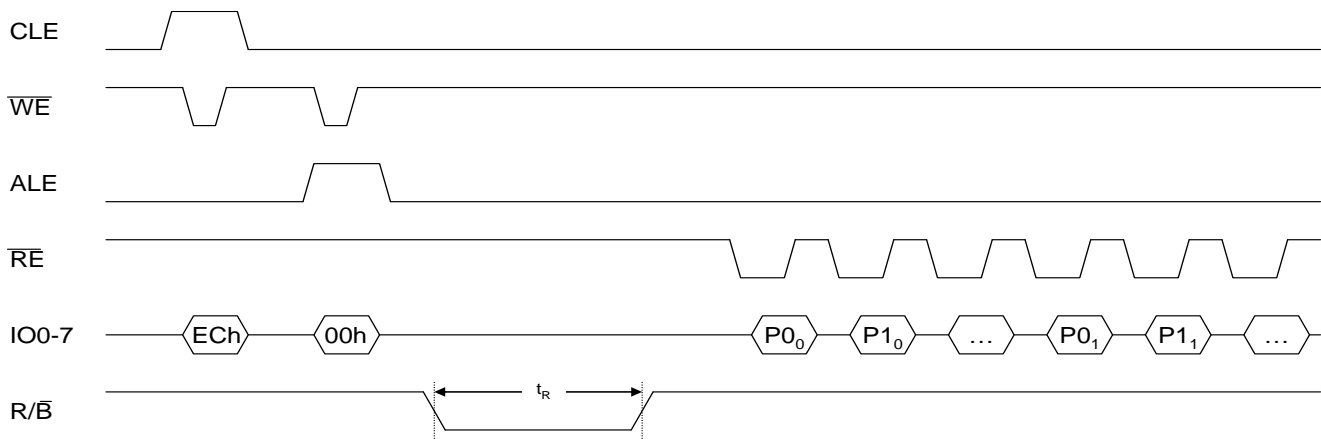
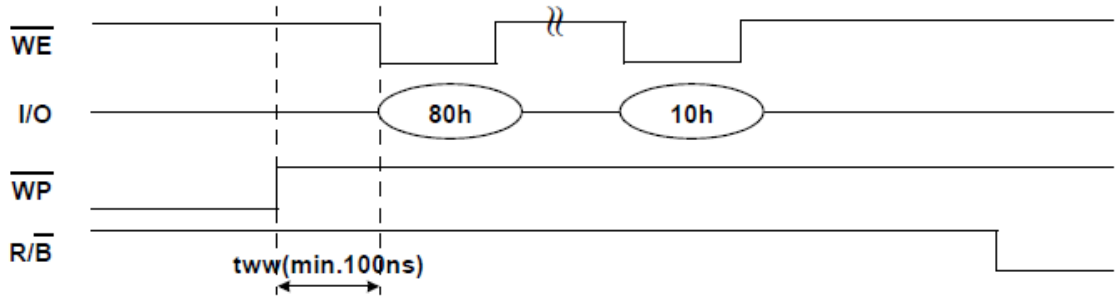


Figure 23 : Read Parameter Page timings

1. Enable Mode



2. Disable Mode

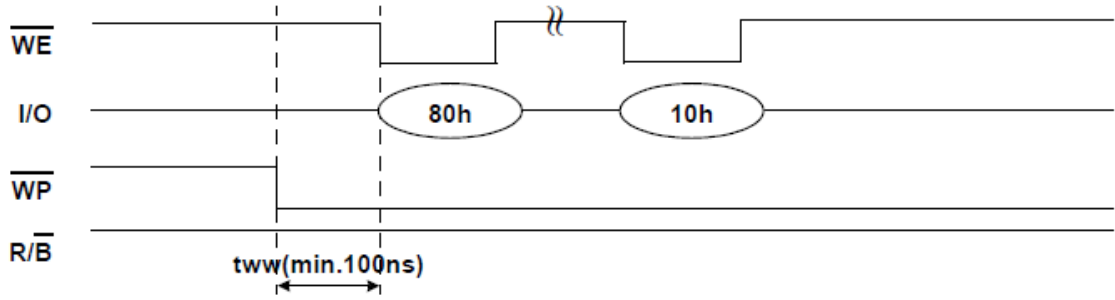
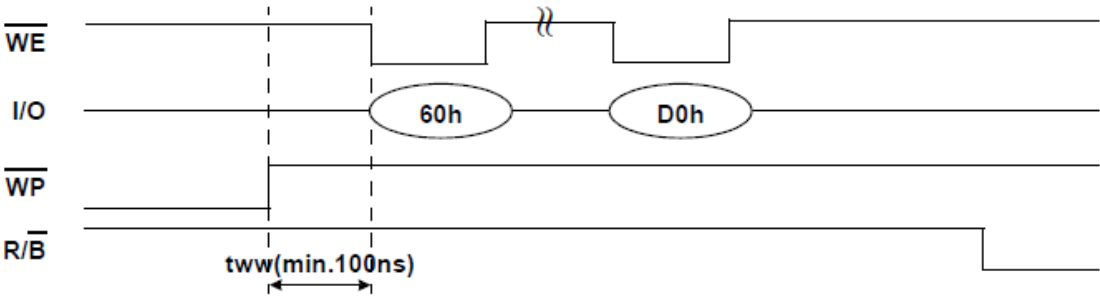


Figure 24 : tWW in Program Operation

1. Enable Mode



2. Disable Mode

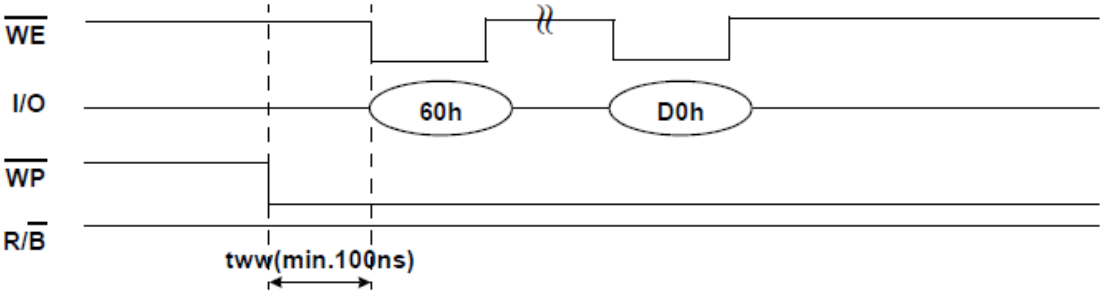
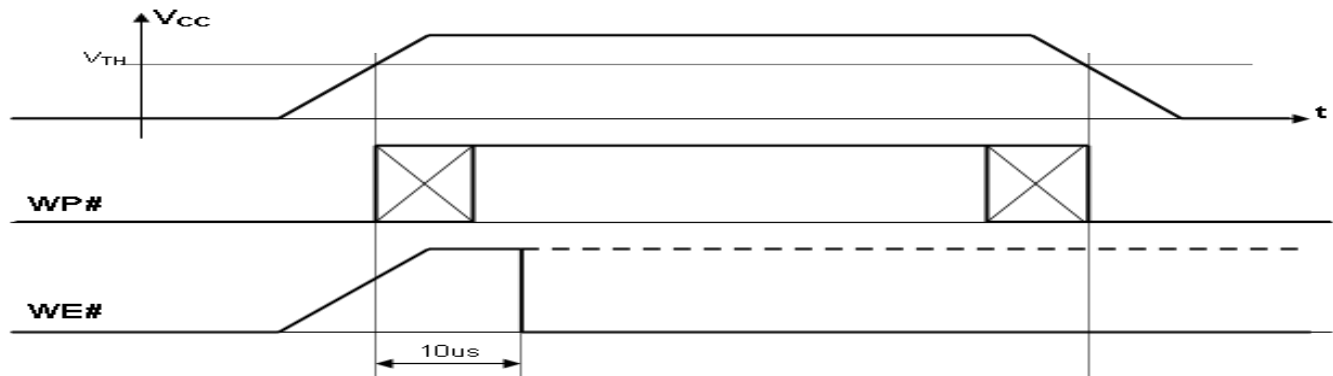
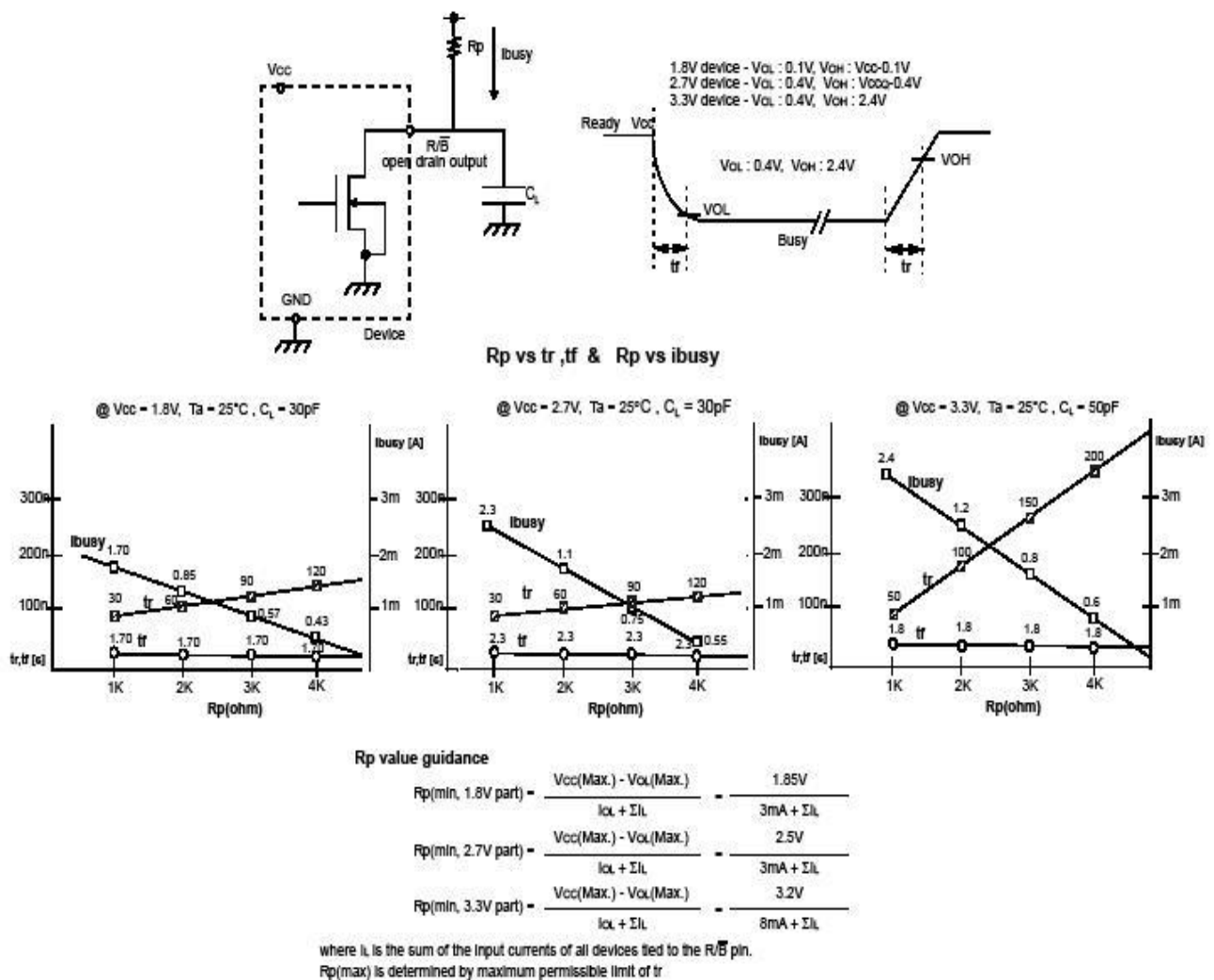


Figure 25 : tWW in Erase Operation

**Note :**  $V_{TH}$  = **1.5** Volt for 1.8 Volt Supply devices; **2.5** Volt for 3.0 Volt Supply devices



**Figure 26 : Power on and Data Protection timings**



**Figure 27 : Ready/Busy Pin electrical application**

## 6 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart

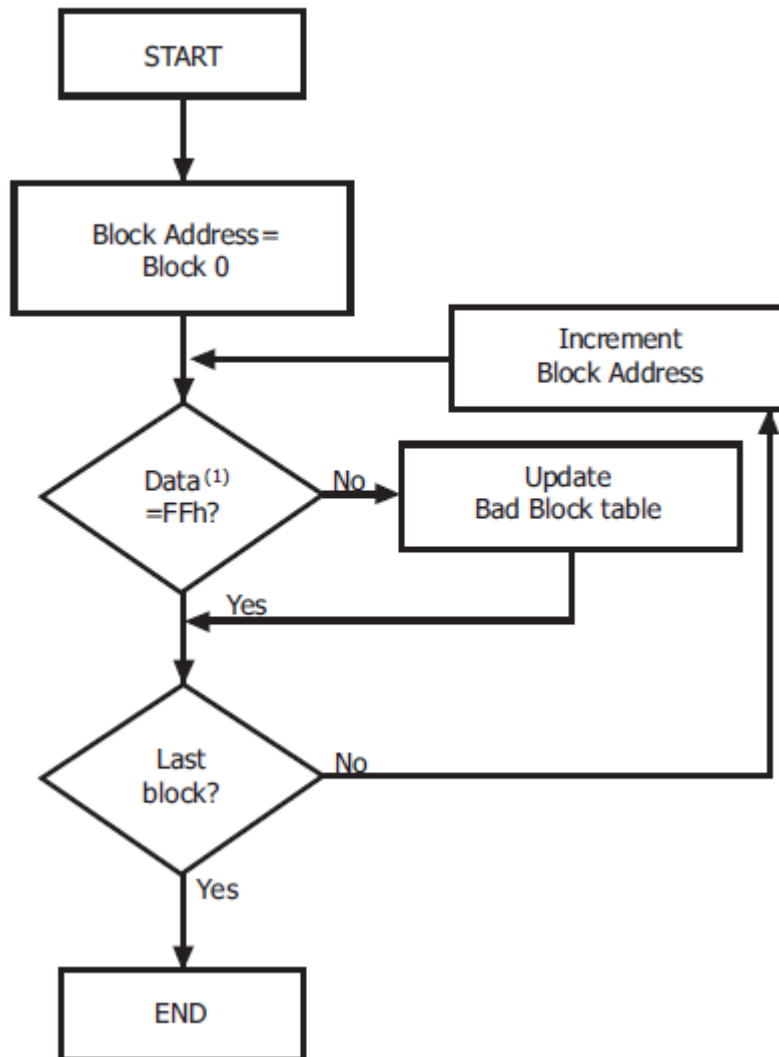


Figure 28 : Bad Block Management Flowchart

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

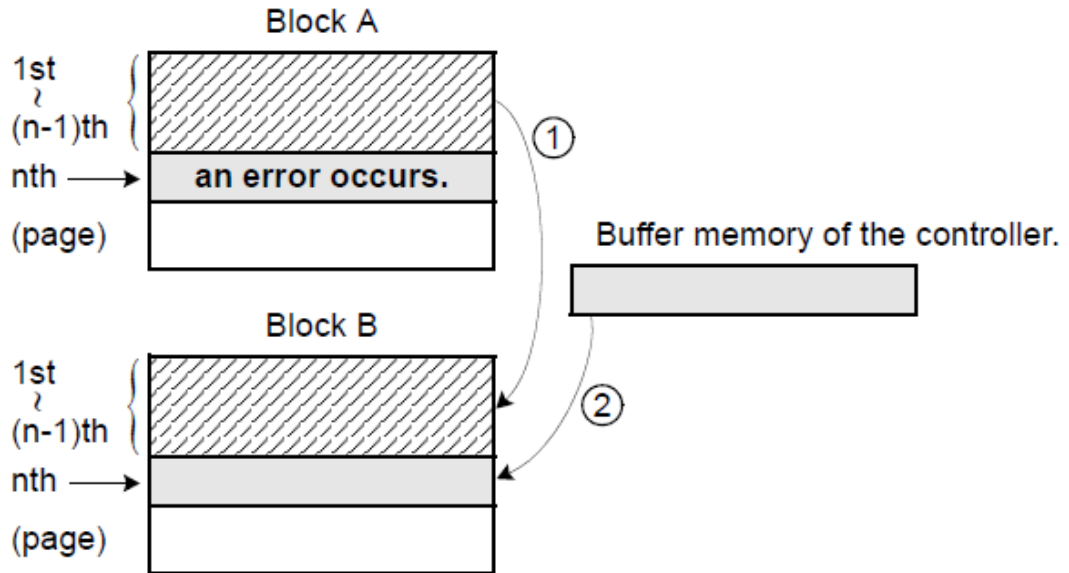
The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

**Figure 29 : Block Failure**

Block Replacement flow is as below

1. When an error happens in the nth page of the Block 'A' during erase or program operation.
2. Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3. Copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4. Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

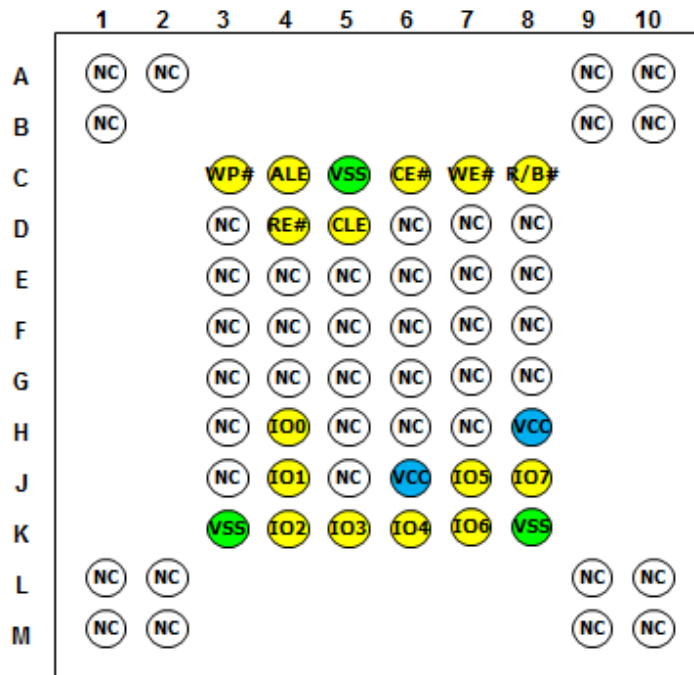


**Figure 30 : Bad Block Replacement**

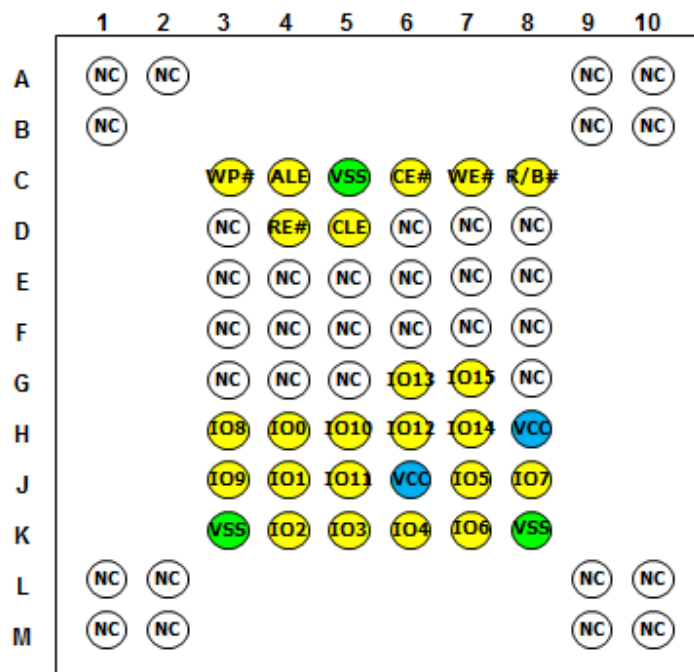


## 7.2 Ball Assignment: 63-Ball FBGA (Balls Down, Top View)

x8



x16



**PACKAGE DIMENSIONS**  
**63-Ball FBGA PACKAGE TYPE**

